CLAIMS

1. A memory circuit for providing word line redundancy in a memory sector during an erase operation, said memory circuit comprising:

said memory sector comprising a plurality of memory cells;

each said plurality of memory cells having a gate connected to a corresponding word line;

each said corresponding word line connected to an output of a corresponding decoding circuit;

each said corresponding decoding circuit receiving a corresponding vertical word line signal, a corresponding global word line signal, and a corresponding sector supply voltage;

said corresponding sector supply voltage being capable of supplying an erase voltage;

each said corresponding decoding circuit further being capable of selectively excluding said corresponding word line from receiving said erase voltage during said erase operation.

2. The memory circuit of claim 1, wherein said corresponding word line is excluded from receiving said erase voltage based upon at least one of said corresponding vertical word line signal and said corresponding global word line signal.

3. The memory circuit of claim 2, wherein said corresponding vertical word line signal can be switched between a negative voltage and zero volts.

4. The memory circuit of claim 2, wherein said corresponding global word line signal can be switched between a positive voltage and a negative voltage.

5. The memory circuit of claim 1, wherein said erase voltage is approximately -9 Volts.

6. The memory circuit of claim 1, further comprising a plurality of local sector supply voltages supplied to said memory sector during said erase operation, said corresponding sector supply voltage corresponding to a first one of said plurality of local sector supply voltages.

7. The memory circuit of claim 6, wherein each of said plurality of local sector supply voltages can be configured to supply either an erase voltage or a non-erase voltage independently of the others of said plurality of local sector supply voltages, wherein said corresponding word line is capable of being excluded from receiving said erase voltage by configuring at least one of said plurality of local sector supply voltages to supply said non-erase voltage.

8. The memory circuit of claim 7, wherein a second word line is supplied said

erase voltage by a second one of said plurality of local sector supply voltages during said erase operation.

9. The memory circuit of claim 7, wherein said non-erase voltage is approximately zero Volts.

10. A memory circuit for providing word line redundancy in a memory sector during an erase operation, said memory sector comprising a plurality of memory cells, each said plurality of memory cells having a gate connected to a corresponding word line, said memory circuit comprising:

voltage supply means for supplying a sector supply voltage, said sector supply voltage being capable of supplying an erase voltage;

decoding means for receiving a vertical word line signal, a global word line signal, and said sector supply voltage;

said decoding means coupled to said corresponding word line;

said decoding means further comprising means for selectively excluding said corresponding word line from receiving said erase voltage during said erase operation.

11. The memory circuit of claim 10, wherein said corresponding word line is excluded from receiving said erase voltage based upon at least one of said vertical word line signal and said global word line signal.

12. The memory circuit of claim 11, wherein said vertical word line signal can be switched between a negative voltage and zero volts.

13. The memory circuit of claim 11, wherein said global word line signal can be switched between a positive voltage and a negative voltage.

14. The memory circuit of claim 10, wherein said erase voltage is approximately -9 Volts.

15. The memory circuit of claim 10, further comprising means for providing a plurality of local sector supply voltages, said plurality of local sector supply voltages supplied to said memory sector during said erase operation, said sector supply voltage corresponding to one of said plurality of local sector supply voltages.

16. The memory circuit of claim 15, wherein each of said plurality of local sector supply voltages can be configured to supply either an erase voltage or a non-erase voltage independently of the others of said plurality of local sector supply voltages, wherein said means for selectively excluding said corresponding word line from receiving said erase voltage comprises configuring at least one of said plurality of local sector supply voltages to supply said non-erase voltage.

17. A memory circuit for providing word line redundancy in a memory sector

during an erase operation, said memory sector comprising a plurality of memory cells; each of said plurality of memory cells having a gate connected to a corresponding word line, each said corresponding word line connected to an output of a corresponding decoding circuit, said memory circuit being characterized by:

each said corresponding decoding circuit receiving a corresponding vertical word line signal, a corresponding global word line signal, and a corresponding sector supply voltage;

said corresponding sector supply voltage being capable of supplying an erase voltage;

each said corresponding decoding circuit further being capable of selectively excluding said corresponding word line from receiving said erase voltage during said erase operation.

18. The memory circuit of claim 17, wherein said corresponding word line is excluded from receiving said erase voltage based upon at least one of said corresponding vertical word line signal and said corresponding global word line signal.

19. The memory circuit of claim 17, further comprising a plurality of local sector supply voltages supplied to said memory sector during said erase operation, said corresponding sector supply voltage corresponding to one of said plurality of local sector supply voltages.

20. The memory circuit of claim 19, wherein each of said plurality of local sector supply voltages can be configured to supply either an erase voltage or a non-erase voltage independently of the others of said plurality of local sector supply voltages, wherein said corresponding word line is excluded from receiving said erase voltage by configuring at least one of said plurality of local sector supply voltages to supply said non-erase voltage.